21152 PCI-to-PCI Bridge Evaluation Board

User's Guide

July 1998

Order Number: 278127-001

Contents

Figures

Tables

Introduction 1

This document describes the Intel 21152 PCI-to-PCI Bridge Evaluation Board (also referred to as the EB152). The EB152 is an evaluation and development board for systems based on the Intel 21152 PCI-to-PCI Bridge chip (the 21152).

Intel's 21152 is a second-generation PCI-to-PCI bridge and is fully compliant with the electrical and protocol requirements of the *PCI-to-PCI Bridge Architecture Specification, Revision 2.1*, and the *PCI-to-PCI Bridge Architecture Specification, Revision 1.0*. The 21152 provides full support for delayed transactions, which enables the buffering of memory read, I/O, and configuration transactions. The 21152 has separate posted write, read data, and delayed transaction queues with significantly more buffering capability than first-generation bridges.

For detailed information about the 21152, refer to the *21152 PCI-to-PCI Bridge Data Sheet.*

1.1 Overview

This chapter provides an overview of the 21152 PCI-to-PCI Bridge Evaluation Board EB152 and includes information about the following topics:

- Jumper location
- Secondary slot numbering and IDSEL mapping
- Typical configurations

The EB152 is a universal PCI expansion board that is used to evaluate the operation of the 21152 in various configurations, and with a variety of PCI devices. The EB152 can be used to perform the following functions:

- Develop initialization code to configure a PCI-to-PCI bridge and the PCI devices behind the bridge
- Evaluate the operation of a PCI-to-PCI bridge with a variety of PCI devices attached to the secondary bus
- Build and evaluate a flexible hierarchy for multiple PCI buses

1.2 Features

The EB152 has the following features:

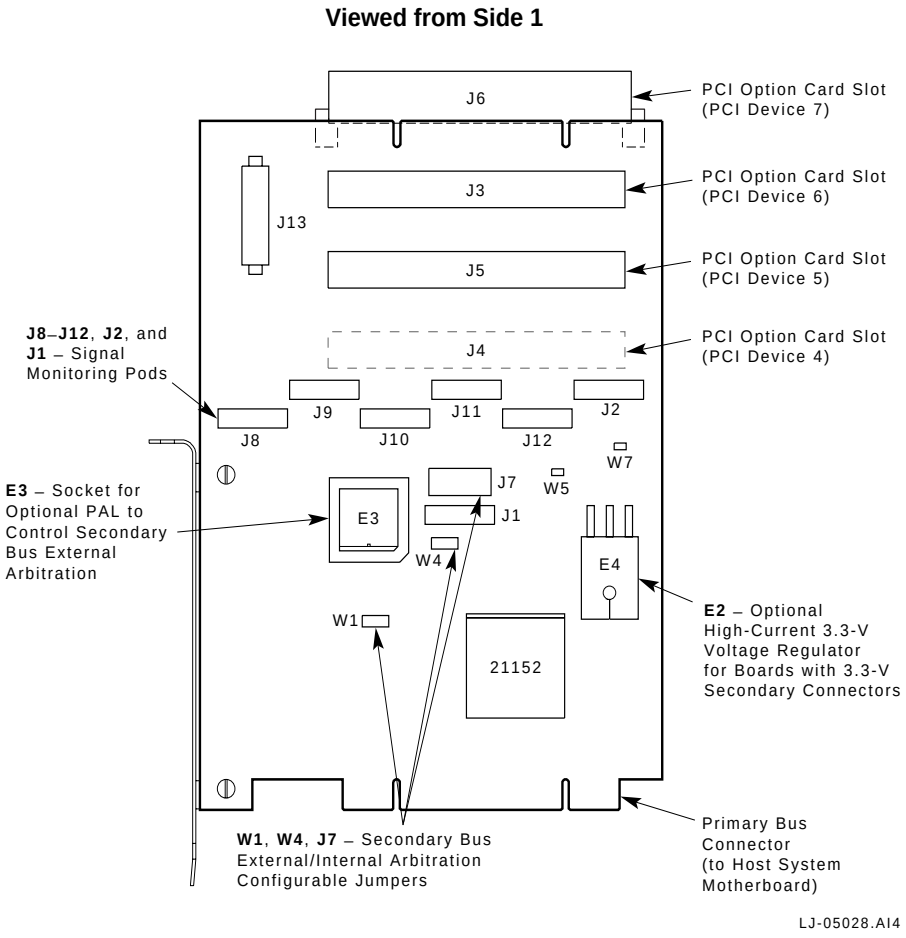
- Complies fully with the protocol and electrical standards of the *PCI Local Bus Specification, Revision 2.1*.
- Includes a 21152 PCI-to-PCI Bridge that provides bridging between a primary and secondary bus.
- Includes a primary PCI bus that plugs into any 5-V or 3.3-V PCI option card slot.

- Supports four secondary 5 V PCI bus option card slots.
- May be built with 3.3-V secondary PCI card slots. If you are interested in this option, call the Intel Information Line (see, Support, Products, and Documentation).
- Supports an optional external secondary bus arbiter.
- Supports multiple levels of PCI bus hierarchy

1.3 Major Components

Figure 1-1 shows the major components on the EB152.

Figure 1-1. EB152 Major Components



1.4 Jumpers

The EB152 provides 10 jumpers that can be used for debugging and for special evaluation tests. The jumpers can be used for monitoring CLK signals and 21152 secondary PCI signals. Additional optional jumpers control secondary bus arbitration.

Table 1-1 shows the connections required to allow observation of these signals at scope pod connector pins.

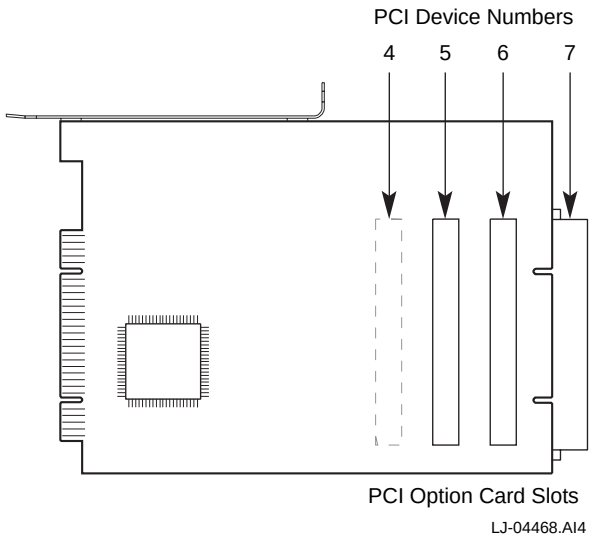
Table 1-1. Jumper Connections

Jumper	Description
J1	This jumper monitors the following signals: **p_clk** (PCI clock) **s_clk_o<4:1>** (four secondary PCI clocks) **s_clk_o<0>** (fed back to the **s_clk** input pin) **s_gnt_l<2>** and **s_gnt_l<3>**.
J2, J8 through J12	Logic analyzer pods can be plugged into these jumpers for monitoring 21152 secondary PCI signals.
W1, W4, J7	These jumpers control secondary bus arbitration. Chapter 4, Secondary Bus Arbitration, provides information about configuring these jumpers.

1.5 Secondary Slot Numbering and IDSEL Mapping

The PCI secondary bus option card slots are mapped to PCI device numbers 4, 5, 6, and 7 as shown in Figure 1-2. The secondary bus lines **s_ad<20:23>** are used as secondary IDSEL lines.

Figure 1-2. Secondary PCI Slot Numbering



1.6 Typical Configurations

The EB152 supports various PCI configurations with different types of devices. Figure 1-3 through Figure 1-6 show examples of PCI configurations.

The primary bus connector attaches to a PCI slot on the motherboard of the host system or to a secondary PCI bus slot on another EB152. A 5-V or universal PCI option card, or another EB152, can be plugged into any one of the four secondary bus option card slots.

Figure 1-3 shows the EB152 with one secondary bus option card.

Figure 1-3. EB152 with One Secondary Bus Option Card

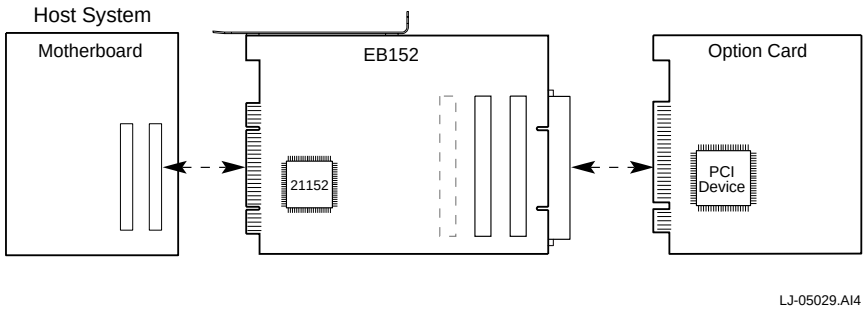


Figure 1-4 shows the EB152 with two secondary bus option cards

Figure 1-4. EB152 with Two Secondary Bus Option Cards

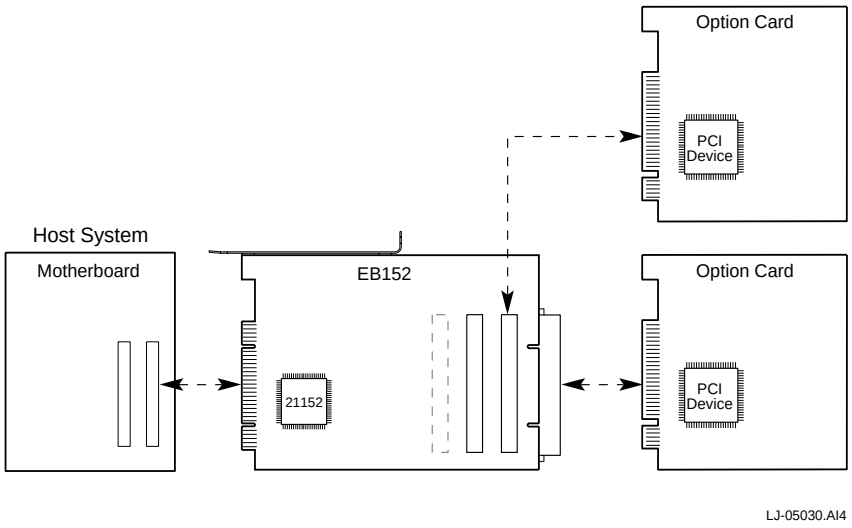


Figure 1-5 shows a tri-level bus with two EB152s.

Figure 1-5. Tri-Level with Two EB152s

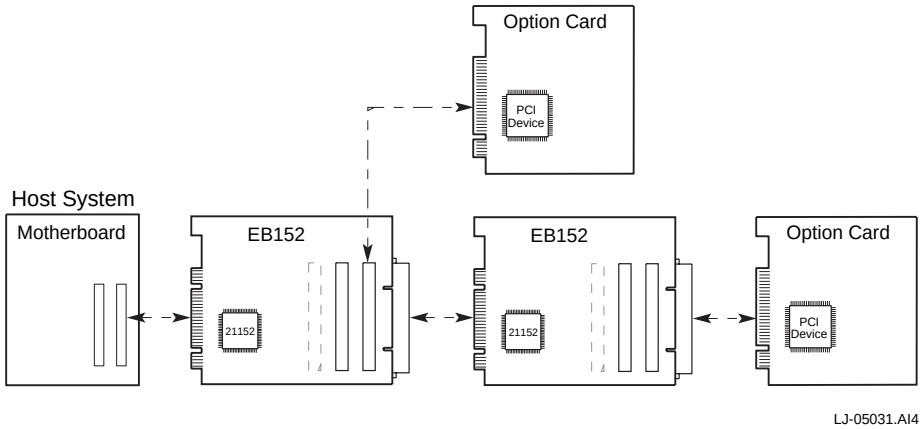
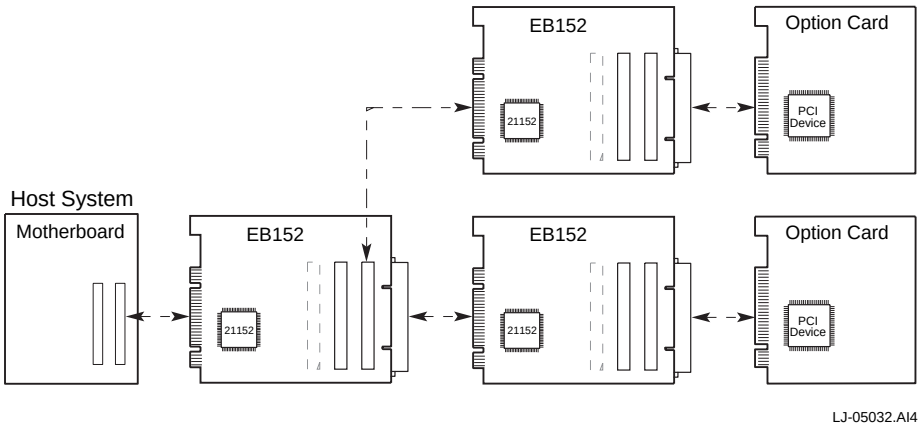


Figure 1-6 shows four PCI buses in a tri-level hierarchy.

Figure 1-6. Four PCI Buses in a Tri-Level Hierarchy



Installation 2

This chapter provides information about the EB152 specifications and the hardware and software requirements for using the EB152. It also describes how to install the EB152.

2.1 Specifications

The physical and power specifications for the EB152 are as follows:

Dimensions:

Height: 20.0 cm (7.90 in)

Width: 13.2 cm (5.20 in)

Power Requirements:

dc amps @ 5 V: 2.0 A (maximum)

2.2 Hardware Requirements

The following equipment is required to use the EB152:

- A computer system equipped with a PCI motherboard
- A PCI expansion slot on the motherboard that is equipped for the 5 V or 3.3 V environment

2.3 Software Requirements

To test the EB152 in x86 DOS or Windows systems, system BIOS must include autoconfiguration code for PCI-to-PCI bridges. If the system BIOS does not include this functionality, contact your BIOS vendor to obtain code with PCI-to-PCI bridge autoconfiguration support.

The EB152 kit provides a DOS utility that can be used to configure the PCI-to-PCI bridge. The diskette included in the EB152 kit contains the DOS utility and a README.TXT file that explains how to use it.

2.4 Installation Procedure

Figure 1-1 illustrates the EB152 and shows the location of components referred to in this section.

Install the EB152 as follows:

1. Power down the host system that will contain the EB152.
2. Place the motherboard with the associated support devices on a bench if mechanical constraints do not allow testing of the EB152 and the expansion slots inside the system box.
3. Configure your system as follows:
   a. Insert the card edge of the EB152 into a PCI slot.
   b. Insert a 5-V or universal option PCI card into any or each of the four secondary bus option card slots. Section 1.4 shows examples of typical PCI configurations.
4. Power up the system.
5. Verify autoconfiguration of the 21152 and of any devices that are plugged in as follows:
   a. Verify that system BIOS or firmware detects and configures the PCI devices downstream of the 21152. If system BIOS is not available, use the DOS utility provided with the EB152 kit to configure the devices downstream of the 21152, and verify proper configuration.
   b. Install device drivers for any PCI devices that are downstream the 21152, and verify proper configuration of those devices.
6. If desired, monitor bridge secondary PCI control signals by connecting a logic analyzer to pods J2 and J8 through J12.

Interrupt Routing 3

This chapter describes the way in which interrupts are routed. This information is provided as a reference for designers.

Because a total of 16 interrupts are connected to the secondary bus PCI slots (INTA#, INTB#, INTC#, and INTD# for each slot) and only four interrupts are driven to the card edge, the 16 incoming interrupts must be combined. This ORing of interrupts is performed in accordance with the *PCI-to-PCI Bridge Architecture Specification*.

Table 3-1 shows the ORing of interrupts.

Table 3-1. Interrupt ORing

Device Number	Interrupt Pin on Device	Interrupt Pin on Board Connector
4	INTA# INTB# INTC# INTD#	INTA# INTB# INTC# INTD#
5	INTA# INTB# INTC# I INTD#	INTB# INTC# INTD# INTA#
6	INTA# INTB# INTC# INTD#	INTC# INTD# INTA# INTB#
7	INTA# INTB# INTC# INTD#	INTD# INTA# INTB# INTC#

In accordance with the *PCI-to-PCI Bridge Architecture Specification, Revision 1.0,* interrupts of the devices on the secondary slots are wire ORed and routed to PCI fingers of the EB152.

Table 3-2 lists the interrupts from the devices on the secondary slots to the interrupts on the EB152 fingers.

Table 3-2. Interrupts from Devices to EB152 Fingers

Interrupts from Devices on Secondary Slots	Interrupts on EB152 Fingers
INTA4 L INTD5 L INTC6 L INTB7 L	INTA L
INTB4 L INTA5 L INTD6 L INTC7 L	INTB L
INTC4 L INTB5 L iNTA6 L INTD7 L	INTC L
INTD4 L INTC5 L INTB6 L INTA7 L	INTD L

Note: In the first column of Table 3-2, the number after each interrupt pin is the device number of the devices in the secondary slots. The L indicates that the assertion level is low.

Secondary Bus Arbitration 4

This chapter describes the use of jumpers to test 21152 secondary bus arbitration, an optional programmable feature. For more detailed information about the 21152 arbiter, refer to the *21152 PCI-to-PCI Bridge Data Sheet.*

The EB152 has two secondary bus arbiter systems:

- An internal arbiter implemented in the 21152 that supports four external masters in addition to the 21152
- An optional external arbiter implemented in an AMD MACH210A programmable device

The default setting is internal arbitration. The internal 21152 arbiter implements a 2-level programmable rotating mode algorithm. Secondary bus parking is done at the last master to use the bus.

The internal arbiter can be disabled, and an external arbiter can be used instead for secondary bus arbitration. The EB152 provides a socket for an optional PAL (labeled E3 in Figure 4-1) to control secondary bus arbitration. If a different external arbiter is used where parking is done at one of the PCI slots, a PCI device must be installed in that slot.To change the default, configure the secondary bus arbiter system using jumpers J7, W4, and W1.

Figure 4-1 shows the location of the arbitration jumpers, and Table 4-1 and Table 4-2 describe their operation.

All jumper positions assume that the EB152 is positioned with the components facing forward and the card edge facing down.

Figure 4-1. Arbitration Jumpers

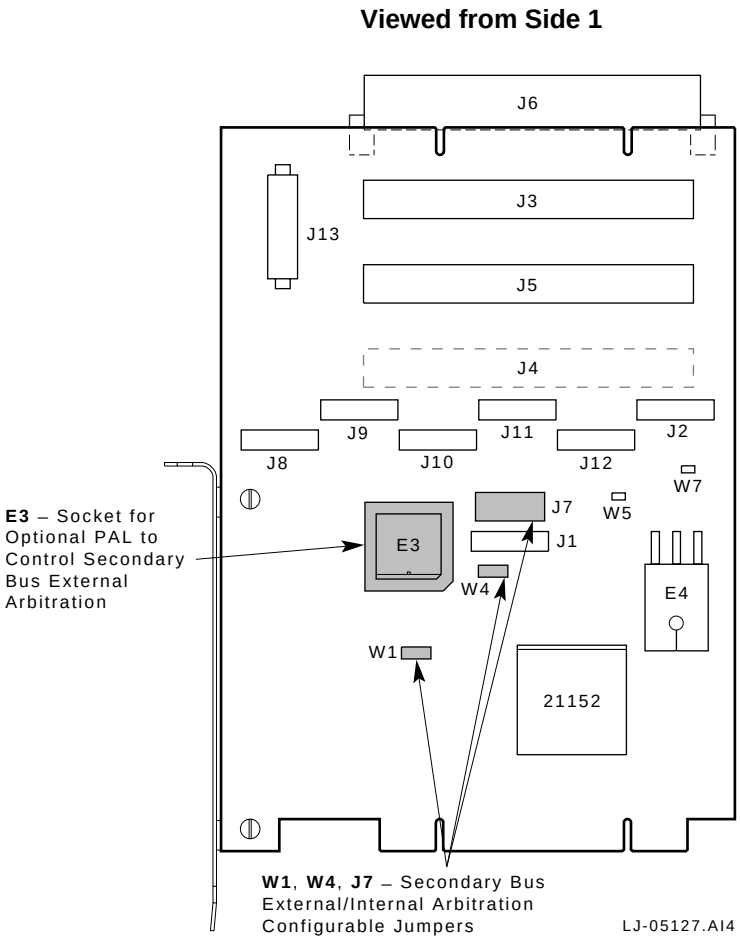


Table 4-1 describes the operation of internal arbitration jumpers.

Table 4-1. Internal Arbitration Jumper Positions

Jumper	Position	Description
J7	Bottom	Selects the 21152 as the source of secondary grant signals.
W4	Left	Selects the board signal **sreq<0>_l** (device 4 request signal) to drive the 21152 **s_req_l<0>** input.
W1	Left	Ties **s_cfn_l** low, which enables the 21152 internal arbiter. When the secondary PCI bus is idle, parking is at the 21152.

Table 4-2 describes the operation of jumpers for external arbitration with PAL.

Table 4-2. External PAL Arbitration Jumper Positions

Jumper	Position	Description
J7	Top	Selects the PAL as the source of secondary grants.
W4	Right	Selects the board signal **gt_out<4>** (the external secondary grant to the 21152) to drive the 21152 **s_req_l<0>** input.
W1	Right	Ties **s_cfn_l** high, which disables the21152 internal arbiter and causes the following reconfigurations: Signal **s_gnt_l<0>** becomes the secondary bus request. Signal **s_req_l<0>** becomes the secondary bus grant. The PAL parks the secondary bus at the 21152.

Kit Contents A

This appendix lists the contents of the Intel Semiconductor 21152 PCI-to-PCI Bridge Evaluation Kit.

The Intel Semiconductor 21152 PCI-to-PCI Bridge Evaluation Kit contains the following materials:

- A Intel Semiconductor 21152 PCI-to-PCI Bridge Evaluation Board (EB152)
- A diskette that contains an MS-DOS utility for configuring the EB152
- A documentation package that includes the following:
  - *21152 PCI-to-PCI Bridge Data Sheet*
  - *21152 PCI-to-PCI Bridge Product Brief*
  - *21152 PCI-to-PCI Bridge Configuration Application Note*
  - *21152 PCI-to-PCI Bridge Hardware Implementation Application Note*
  - *21152 PCI-to-PCI Bridge Evaluation Board User's Guide*
  - *21152 Evaluation System BIOS Letter*
  - 21152 PCI Evaluation Board Schematics
  - 21152 Evaluation Board Vendor Parts List
  - SPICE model kit containing a Level 28 21152 SPICE model and application note
  - Warranty Agreement/Registration Card

Support, Products, and Documentation

If you need technical support, a *Product Catalog*, or help deciding which documentation best meets your needs, visit the Intel World Wide Web Internet site:

http://www.intel.com

Copies of documents that have an ordering number and are referenced in this document, or other Intel literature may be obtained by calling **1-800-332-2717** or by visiting Intel's website for developers at:

http://developer.intel.com

You can also contact the Intel Massachusetts Information Line or the Intel Massachusetts Customer Technology Center. Please use the following information lines for support:

For documentation and general information:	
Intel Massachusetts Information Line	
United States:	1–800–332–2717
Outside United States:	1–303-675-2148
Electronic mail address:	techdoc@intel.com

For technical support:	
Intel Massachusetts Customer Technology Center	
Phone (U.S. and international):	1–978–568–7474
Fax:	1–978–568–6698
Electronic mail address:	techsup@intel.com